



Sheet 1 of 2

Form PTOL-1449 U.S. Department of Commerce
(Rev. 08-98) Patent and Trademark Office

Attorney Docket No.: 0321.67421

Serial No.: 10/787,070

INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Applicant: Andrew B. Kahng et al.

Filing Date: February 25, 2004

Group: 2825

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	International Technology Roadmap for Semiconductors, December 2001 http://public.itrs.net/
JJA	Y. Cao., P. Gupta, A.B. Kahng, D. Sylvester and J. Yang, "Design Sensitivities to Variability: Extrapolations and Assessments in Nanometer VLSI", <i>IEEE International ASIC/SOC Conference</i> , 2002, pp. 411-415.
	"The Outlook for Semiconductor Processes and Manufacturing Technologies in the 0.1- μ m Age", (2001) http://www.cyberfab.net/events/013mmts/links013.html .
	M.L. Rieger, J.P. Mayhew and S. Panchapakesan, "Layout Design Methodologies for Sub-Wavelength Manufacturing", <i>Proceedings of Design Automation Conference</i> , 2001, pp. 85-92.
	Chiang Yang, "Challenges of Mask Cost and Cycle Time", <i>SEMATECH: Mask Supply Workshop, Intel</i> , 2001.
	W. Carpenter, "International SEMATECH" A Focus on the Photomask Industry http://www.kla-tencor.com/company_info/magazine/autumn00/Inter_SEMATECH_photomaskindustry_AutumnMag00-3.pdf (2000)
	B. Bruggeman et al., "Microlithography Cost Analysis", <i>Interface Symposium</i> , 1999.
	S. Murphy, Dupont Photomask, <i>SEMATECH: Mask Supply Workshop</i> , 2001.
	A. Agarwal, D. Blaauw and V. Zolotov, "Statistical Timing Analysis Using Bounds and Selective Enumeration", <i>ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of digital Systems</i> , 2002, pp. 1243-1260.
	Robert R. Kinnison, <i>Applied Extreme Value Statistics</i> , Battelle Press, 1985.
JJA	W. Chuang, S.S. Sapatnekar and I.N. Hajj, "Delay and Area Optimization for Discrete Gate Sizes under Double-Sided Timing Constraints", <i>Proc. IEEE Custom Integrated Circuits Conference</i> , 1993, pp. 9.4.1-9.4.4.

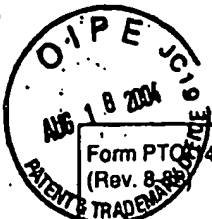
Examiner

Date Considered

10-26-05

*Examiner:

Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-449 U.S. Department of Commerce
(Rev. 8-88) Patent and Trademark Office

Attorney Docket No.: 0321.67421

Serial No.: 10/787,070

INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Applicant: Andrew B. Kahng et al.

Filing Date: February 25, 2004

Group: 2825

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JR	R. Nair, C.L. Berman, P.S. Hauge and E.J. Yoffa, "Generation of Performance Constraints for Layout" <i>IEEE Transactions on Computer Aided Design</i> , 8(8), 1989, pp. 860-874.
JR	A.E. Dunlop, J.P. Fishburn, D.D. Hill and D.D. Shugard, "Experiments using Automatic Physical Design Techniques for Optimizing Circuit Performance", <i>Proc. IEEE International Symposium on Circuits and Systems</i> , (2), 1990, pp. 847-851.
JR	M. Sarrafzadeh, D.A. Knol and G.E. Tellez, "A Delay Budgeting Algorithm Ensuring Maximum Flexibility in Placement", <i>IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems</i> , 16(11), 1997, pp. 1332-1341.
	Synopsis Design Compiler, http://www.synopsys.com/products/logic.html

Examiner James Sun LinDate Considered 10-26-05

*Examiner:

Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.